Analysis of Interface Traps in Electronic Devices

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Introduction

- Interface traps play an important role in semiconductor devices which are found in all electronic equipment.
- These traps directly affect the speed of the charge carriers in the semiconductors, and therefore the device speed.
- To optimise device performance, factors affecting interface traps need to be understood and accurately measured.

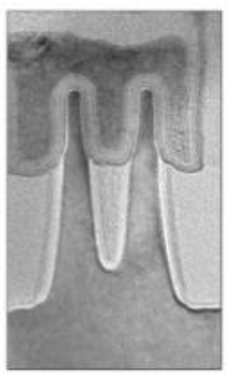


Fig. 1(a) – Enlarged view of the actual device.

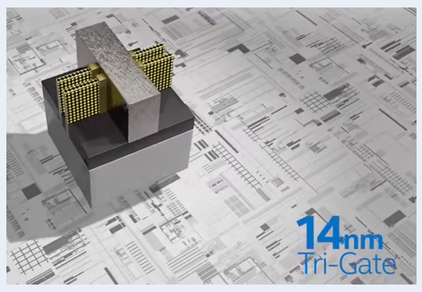


Fig. 1(b) – Structural representation of the device.

14nm Tri-gate technology currently being used by Intel.

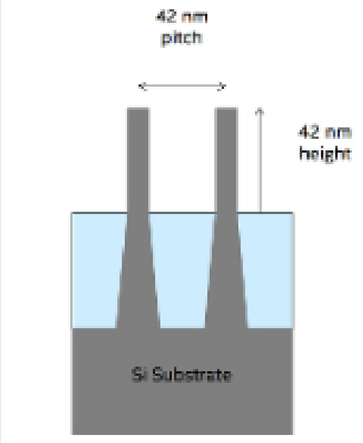


Fig. 1(c) – Design parameters of the device

Aim

- This project is aimed at comparing and measuring the accuracy of different techniques for determining the interface trap density (Dit) found within thin dielectric layers (2-3nm thick) in state-of-the-art electronic devices.
- To develop an automated software which enables fast and easy analysis of experimental data.

Interface Traps

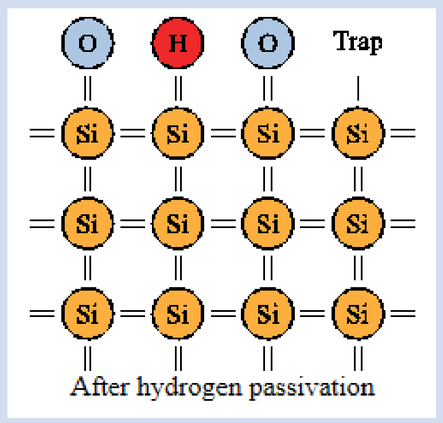
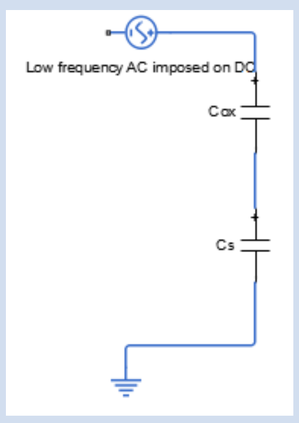
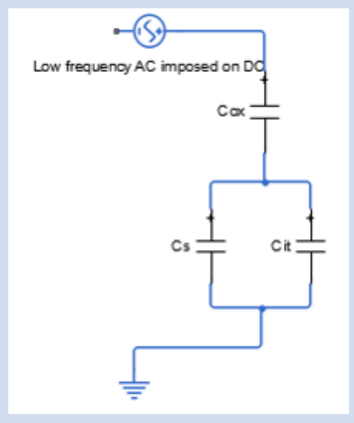


Fig. 2(a) – Representation of Interface traps



(b)



(c)

Fig. 2 – (b)Low frequency (c)High frequency circuit representation of Interface traps

Results

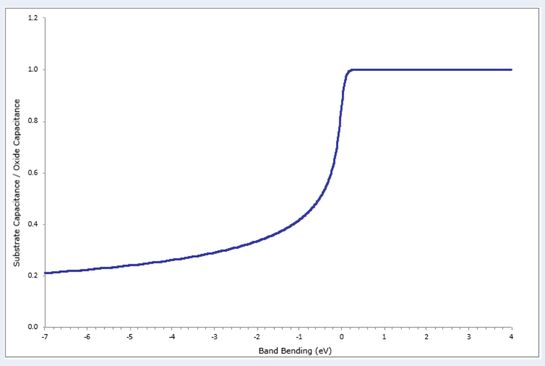


Fig. 3(a) – Simulated CV Curve

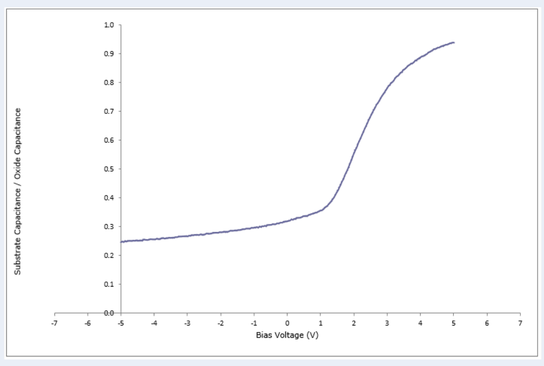


Fig. 3(b) – Experimental CV Curve

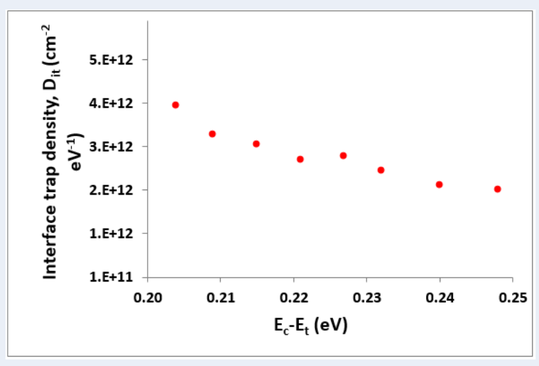


Fig. 3(c) – Interface Trap Density obtained by Terman's Method

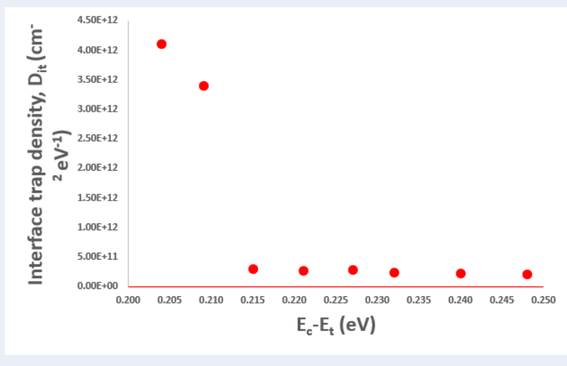


Fig. 3(d) – Interface Trap Density obtained by High-Low CV Method

Process

Current Stage of the Project

Summary

- Automated software was developed for faster Dit calculations.
- Comparisons (based on accuracy and usability) between the Terman and High-Low CV method was made. A documentation highlighting the same was also prepared.

Future Work

- Develop the Graphical User Interface (GUI).
- Make the software more user friendly for those without a programming background.

Reference

Image Source - Figure 1 (a)-(c): www.intel.com